Claim Amendments

The following complete listing of the claims including amended claims will replace all prior versions of claims in the application.

Listing of Claims

1. (currently amended) A processor comprising a programmable pipeline and at least one interface engine ~~(130)~~, adapted to be connected to at least one external device (140) located externally of the processor, ~~characterized in that~~ wherein the interface engine ~~(130)~~ is adapted

- to receive a request ~~(170)~~ from the programmable pipeline,
- to send to the external device ~~(140)~~ a request output ~~(270)~~, based at least partly on the request ~~(170)~~,
- to receive an external reply ~~(330)~~ from the external device ~~(140)~~, and
- to send to the pipeline a response ~~(340)~~, based on the external reply ~~(330)~~, to the request ~~(170)~~.

2. (currently amended) A processor according to claim 1, whereby the request ~~(170)~~ comprises a first request code ~~(210)~~, according to a first coding scheme, the interface engine ~~(130)~~ being adapted to execute a program, the execution being dependent upon the first request code ~~(210)~~, and to obtain, as a result of the execution of the program, at least one device control code ~~(300)~~, according to a second coding scheme, in addition to which the interface engine ~~(130)~~ is adapted to send the device control code ~~(300)~~ to the external device (140), or the request output ~~(270)~~ is based at least partly on the device control code ~~(300)~~.

3. A processor according to claim 2, whereby the device control code is an operational code of the external device.

4. (currently amended) A processor according to claim 2 ~~or 3~~, whereby the program is stored in a microcode memory ~~(230)~~ included in the interface engine.

5. (currently amended) A processor according to ~~any of the claims 1 to 4~~ claim 1, whereby the pipeline comprises a plurality of access points, and the interface engine ~~(130)~~ is adapted to receive a request ~~(170)~~ from at least one of the access points ~~(150)~~, the interface engine comprising a reply control unit ~~(320)~~ adapted to receive at least one receiver ID signal ~~(213)~~ related to the request ~~(170)~~, and to determine, based on the receiver ID signal ~~(213)~~, the access point which is to receive the response ~~(340)~~.

6. (currently amended) A processor according to claim 5, whereby the reply control unit ~~(320)~~ is adapted to receive an input control signal (310), based on which timing information for receiving the external reply ~~(330)~~ from the external device ~~(140)~~ can be determined.

7. (currently amended) A processor according to ~~any of the claims 1 to 6~~ claim 1, at which the pipeline comprises a plurality of access points, whereby the number of access points ~~(150)~~ adapted to send a request to the interface engine ~~(130)~~ can be adjusted.

8. (currently amended) A method in processor comprising a programmable pipeline and at least one interface engine ~~(130)~~, adapted to be connected to at least one external device ~~(140)~~ located externally of the processor, ~~characterized in that it comprises~~ wherein the method comprising the steps of

- receiving a request ~~(170)~~ from the programmable pipeline,

- sending to the external device ~~(140)~~ a request output ~~(270)~~, based at least partly on the request ~~(170)~~,
- receiving an external reply ~~(330)~~ from the external device ~~(140)~~, and
- sending to the pipeline a response ~~(340)~~, based on the external reply ~~(330)~~, to the request ~~(170)~~.

9. (currently amended) A method according to claim 8, wherein the request ~~(170)~~ comprises a first request code ~~(210)~~, according to a first coding scheme, the method further comprising the step of executing a program, the execution being dependent upon the first request code ~~(210)~~, to obtain at least one device control code ~~(300)~~, according to a second coding scheme, in addition to which the device control code ~~(300)~~ is sent to the external device ~~(140)~~, or the request output ~~(270)~~ is based at least partly on the device control code ~~(300)~~.

10. (currently amended) A method according to claim 9, whereby the device control code ~~(300)~~ is an operational code of the external device.

11. (currently amended) A method according to claim 9 ~~or 10~~, whereby the program is stored in a microcode memory ~~(230)~~ included in the interface engine.

12. (currently amended) A method according to ~~any of the claims 8 to 11~~ claim 8, at which the pipeline comprises a plurality of access points, whereby the request ~~(170)~~ is received from at least one of the access points ~~(150)~~, the method further comprising the steps of

- sending at least one receiver ID signal ~~(213)~~, related to the request ~~(170)~~, to a re-ply control unit ~~(320)~~ included in the interface engine, and
- determining, based on the receiver ID signal ~~(213)~~, the access point which is to receive the response ~~(340)~~.

13. (currently amended) A method according to claim 12, further comprising the step of sending to the reply control unit ~~(320)~~ an input control signal ~~(310)~~, based on which timing information for receiving the external reply ~~(330)~~ from the external device ~~(140)~~ can be determined.

14. (currently amended) A method according to ~~any of the claims 8 to 13~~ claim 8, at which the pipeline comprises a plurality of access points, whereby the number of access points ~~(150)~~ adapted to send a request to the interface engine ~~(130)~~ can be adjusted.